IN THE CLAIMS:

1. A method of fabricating an integrated circuit, comprising the steps of:

forming a dielectric layer over a semiconductor body;

forming a hole in said dielectric layer;

depositing a metal layer over said dielectric layer including in said hole using physical vapor deposition;

performing a sputter etch using a low bias after said step of depositing the metal layer; and

depositing a metal filler to fill said hole.

2. The method of claim 1, wherein said hole comprises a trench.

3. The method of claim 1, wherein said hole comprises a via.

4. The method of claim 1, wherein said hole comprises a contact.

5. The method of claim 4, wherein said metal layer comprises a liner/barrier material and said metal filler comprises tungsten.

6. The method of claim 1, wherein said metal layer comprises a liner/barrier material.

7. The method of claim 6, wherein said liner/barrier material is selected from the group consisting of Ti, TiN, Ta, TaN, WN, TiNSi, TaNSi, MoN.

8. The method of claim 1, wherein said metal layer comprises a liner/barrier material and a seed layer.

9. The method of claim 8, wherein said liner/barrier material comprises TaN and said seed layer comprises copper.

10. The method of claim 1, wherein said step of depositing a metal layer forms an overhang portion at upper corners of said hole and wherein said sputter etch step reduces a thickness of said overhang portion.

11. The method of claim 1, wherein said low bias is in the range of 0 to –300 volts.

12. A method of fabricating an integrated circuit, comprising the steps of:

forming a dielectric layer over a semiconductor body;

forming a trench in a first part of said dielectric layer;

forming a via in a second part of said dielectric layer;

depositing a liner/barrier layer over said dielectric layer including in said trench and in said via using physical vapor deposition (PVD);

performing a sputter etch using a low bias after said step of depositing a liner/barrier layer;

depositing a seed layer over said liner/barrier layer; and

depositing a copper layer over said seed layer.

13. The method of claim 12, wherein said step of depositing a seed layer comprises PVD and occurs prior to said step of performing a sputter etch.

14. The method of claim 12, wherein said steps of forming the liner/barrier layer and forming the seed layer create an overhang portion of liner/barrier and seed material and wherein said sputter etch step reduces thickness of said overhang portion.

15. The method of claim 12, wherein said liner/barrier layer comprises a material selected from the group consisting of Ti, TiN, Ta, TaN, TiNSi, WN, TaNSi, MoN.

16. The method of claim 12, wherein said low bias is in the range of 0 to –300 volts.

17. A method of fabricating an integrated circuit, comprising the steps of:

forming a pre-metal dielectric (PMD) layer over a semiconductor body;

forming a contact hole in said PMD layer;

depositing a liner layer over said PMD layer including in said contact hole using physical vapor deposition, wherein said liner layer has an overhang portion at a top of said contact hole;

performing a sputter etch using a low bias to at least reduce a thickness of said overhang portion;

depositing a barrier layer over said liner layer; and

depositing a metal filler to fill said contact hole.

18. The method of claim 17, wherein said step of depositing a barrier layer comprises PVD and occurs prior to said step of performing a sputter etch.

19. The method of claim 17, wherein said metal filler comprises tungsten.

20. The method of claim 17, wherein said metal filler comprises CVD TiN.

21. The method of claim 17, wherein said liner layer comprises Ti and barrier layer comprises TiN.

22. The method of claim 17, wherein said low bias is in the range of 0 to –300 volts.